

December 10, 2003

To: Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/661,042 09/12/03

Tzong Shi Jan

A MULTI-LAYERED METAL ROUTING TECHNIQUE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

12/19/0

TSMC-02-096

- U.S. Patent 5,987,241 to Goldberg et al., "Routing Techniques to Assure Electrical Integrity in Datapath Blocks," discloses routing techniques.
- U.S. Patent 5,990,502 to Park, "High Density Gate Array Cell Architecture with Metallization Routing Tracks Having a Variable Pitch," discloses an architecture with metallization routing tracks.
- U.S. Patent 6,091,090 to Gheewala, "Power and Signal Routing Technique for Gate Array Design," discloses a power and signal routing technique.
- U.S. Patent 5,923,089 to Yao et al., "Efficient Routing Method and Resulting Structure for Integrated Circuits," discloses a routing method.
- U.S. Patent 5,923,059 to Gheewala, "Integrated Circuit Cell Architecture and Routing Scheme," reveals a cell and routing scheme.

Sincerely

Stephen B. Ackerman, Reg. No. 37761

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.